

# **VCPU R1**

VCPU programmer's documentation

V0.999

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# 1 Introduction

## 1.1 Goals

The goal of the Flexible SD drive *firmware*<sup>1</sup> (FlexSD fw. in short) VCPU<sup>2</sup> extension is to make the SD2IEC<sup>3</sup> drive capable of executing downloaded programs like the classic Commodore disk drives. SD2IEC is a drive family with different hardware. With VCPU the executed program uses a unified (virtual) hardware so separate support is no longer needed. **Compatibility with existing older drives is not a goal!** VCPU is not limited to regular disk images, it can use all of the functions of the drive so a much larger storage becomes available to the computer than the old disk drives. In addition any data transfer protocol can be implemented to fulfill the requirements of the programmer.

## 1.2 Differences compared to programming the original Commodore drives

Programming the drive's VCPU requires a bit different logic than the direct hardware programming of the Commodore drives. Accessing the direct storage device is limited. The usable commands the computer can send over the serial bus are the same but during VCPU execution the program "moves" to the drive memory where the results of the executed tasks are stored too. The only "near-hardware" task is communication with the computer; VCPU provides special instructions for this.

## 1.3 License

Both *FlexSD firmware* and it's VCPU extension are licensed under GPLv2. So using parts or whole of the firmware must be in accordance with this license. But this license does not apply to programs executed by the VCPU! The programmer can choose whatever license he/she wants for the executed programs<sup>4</sup>.

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1 **Flexible SD drive firmware (FlexSD fw)** is an **sd2iec firmware** fork. (The original can be found at <https://sd2iec.de>) In this documentation the term firmware means **FlexSD firmware**.

2 VCPU: "Virtual CPU". Most of these drives are built on a microcontroller (an integrated circuit containing a CPU, data- and program memory and peripherals - so in fact a complete computer) which can execute command only from ROM. It's RAM can contain data only! The VCPU is a software CPU implementation running in the microcontroller ROM which executes the program copied to RAM.

3 In this documentation the name **SD2IEC** refers to the hardware. These are the same as the supported hardware by the original *sd2iec firmware*.

4 The programmer must be aware that the program is inspected and processed by a software and there is no protection mechanism against deciphering them.

## 2 Commands available for the computer

To program the SD2IEC drive several new commands are required which makes the VCPU functions available to the computer. These commands (with the help of the KERNAL) can be executed in the usual way by sending them over the “command channel” and the responses can be read from the “error channel”. (The programming is the same as for the traditional CBM drives, details can be found in the well known documentations.)

The VCPU extension commands follows “**Zx**” form. To an unknown VCPU command the drive will respond with a “35, SYNTAX ERROR, 00, 00” error message.

### 2.1 “ZI”: Query VCPU information

The result is 4 BYTEs long:

1. VCPU version which is made of two parts: B5..0<sup>5</sup>: the version itself (currently \$1<sup>6</sup>), B7..5: device bus type. (Currently \$2: CBM SERIAL. Reserved type codes: \$1: IEEE-488, \$3: CBM FAST SERIAL, \$4: TCBM.)
2. Size of “command channel” in BYTEs. This is usually 120, there is no lesser value present. The computer can write this many BYTEs to the drive in the “command channel”!
3. Size of “error channel” in BYTEs. This is usually 100, there is no lesser value present. The drive can send this many BYTEs to the computer in the “error channel”!
4. Number of data buffers. This is 6 or more (maximum 15). The drive will reserve this many buffers of 256 BYTEs. This is actually the memory size of the VCPU, the usable program memory. (6×256 = 1.5 KBYTE, 15×256 = 3.75 KBYTE.)

Returned VCPU version is currently \$41. (%010 and %00001.) If the drive does not have a VCPU extension it will return “30, SYNTAX ERROR, 00, 00” error message. In this response the first BYTE is always \$33 (ASCII code of “3”). VCPU version BYTE will never have a value of \$33 so this can be used easily to detect the presence of the expansion in the drive *firmware*. (Checking for the presence of VCPU this command is the recommended. The drive – normal / short – version string characters does not necessarily refer to VCPU support, they may change in the future!)

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5 Designation of bits in a BYTE is “**B**” + number of bit. In case of multiple bits the range is specified! (**B5..0**)  
Numbering of the bits is the usual: the least significant bit is 0 (**B0**), the most significant is 7 (**B7**).

6 In this documentation the number systems follow the convention of 6502 *assemblers*: hexadecimal numbers are marked with prefix “\$”, binaries are marked with prefix “%”. Numbers without prefix are interpreted in decimal number system.

## 2.2 “ZB”: Query data buffer state

The response is 2 BYTEs for all usable data buffers in the device:

1. Data buffer in use marker, bit 0 (B0) with value %1 marks a used buffer, %0 marks free. Other bits can be used in drive *firmware* but their meaning is irrelevant here. (Meaning of bits other than B0 can change in the future so their value must be ignored!)
2. The channel number belonging to the data buffer (Parameter 3 of OPEN statement, the “secondary address”) used by the computer. This is only valid when the buffer is in use. (B0 of the previous BYTE = %1)! Value is between 0..14 is the data buffer is used for normal file operations. Drive *firmware* can allocate buffers for special uses. In this case their channel number will be outside of this range.

The above two BYTEs are repeated in the response as many times as many data buffers the drive has.

## 2.3 “ZR”+ADDRLO+ADDRHI+LENGTH: Read data buffers as memory

This is the equivalent of the “M-R” command of the 15x1 drives but this one is limited to data buffers only so not all of the SD2IEC drive memory can be read. Size of memory read (with a single command) is limited by the size of the “error channel”. Attempting to read more will result in error! (“35, SYNTAX ERROR, 01, 00”) Omitting “LENGTH” parameter will result in reading 1 BYTE. If the read refers to an address outside the usable memory range it will result in an error too! (“35, SYNTAX ERROR, 02, 00”)

## 2.4 “ZW”+ADDRLO+ADDRHI+BYTE1+...: Write data buffers as memory

Similar to the “M-W” command of 15x1 drives. Memory beginning from the specified address will be written with as many BYTEs as many are present in the package. (The command does not have a size parameter unlike the “M-W” command!). Number of writable BYTEs are limited by the size of the “command channel”, the whole memory write command must fit into it! If an address outside the usable memory range is specified an error will be returned (“35, SYNTAX ERROR, 03, 00”). After a successful write the response will be “00, OK, 00, 00”.

## 2.5 “ZE”+ADDRLO+ADDRHI+...: Execute program using VCPU

With parameters after the “ZE” command not only the start address but all of the VCPU registers can be set. When no parameters specified (not even a start address) the execution will resume with the actual state from the actual position. Parameters can be found at command “ZC”. The response (and the possibility of query) depends on the executed program, it can return anything.

WARNING: the time elapsed between issuing the command “ZE” and the start of the VCPU program execution is not guaranteed, it can depend on the type of the drive and other circumstances. Because of this it’s recommended to implement some kind of synchronization which “notifies” the computer that the drive side code has started. (For example it can generate an impulse on some of the lines of the serial bus and the computer waits for that.)

## 2.6 “ZC”: Query VCPU state

This command returns the (current) state of the VCPU:

- **PCL + PCH**: two BYTEs for current PC position
- **A**: Accumulator
- **X**: X index register
- **Y**: Y index register
- **SR**: status register
- **SP**: stack pointer
- **SPH**: stack pointer upper bits (B15..8)
- **ZPH**: zero page upper bits (B15..8)
- **INT**: interrupt code
- **FUNCT**: code of the called function
- **LASTOP**: code of last executed instruction

In command “ZE” the parameters are from **PCL** to **ZPH** are these values in this order. If no address specified the execution will start from the address that is resulted here. **INT** / **FUNCT** / **LASTOP** values can be used for troubleshooting.

## 3 The VCPU

### 3.1 Major differences

VCPU consists of a software implemented 6502 emulator and a connected (also emulated) hardware. 6502 emulation is not complete, there are some missing and some additional functions:

- Cycle exact execution was not a goal; current implementation executes programs at about the speed of a 1 MHz 6502. (Some instructions are faster, others are slower.)
- “Undocumented” instructions of the original MOS 6502 are not supported! When these opcodes are encountered the execution will be interrupted with an error code. (However some of these opcodes are assigned to new instructions those will execute their proper function.)
- BCD mode is not implemented! CLD instruction is equivalent to NOP, SED is “illegal”.
- Traditional interrupt handling is missing. SEI instruction is NOP, CLI is “illegal”. But RTI is implemented, can be used in the usual way.
- Program execution is possible only from memory assigned to RAM! This memory is the address range \$0000..\$05FF of the emulated 6502 for 6 data buffers and \$0000..\$0EFF for 15 buffers. Jumping outside this range will interrupt the execution with an error code!
- JMP (\$xxFF) instruction works as expected, the buggy operation of the original 6502 is not implemented. Target address of the indirect jump must reside in the RAM area too!!
- BRK instruction is used for system calls but those are not executed by the CPU emulation. Because of this the stack operations of BRK are not implemented.

### 3.2 VCPU extended functions

This functions are not supported by the original 6502!

- **SPH** register: the stack pointer (**SP**) of the 6502 is 8 bits, upper 8 bits are always \$01. In VCPU this is stored in register **SPH**, so the stack can be relocated to an other memory page. Over- or underflow of the 8 bits **SP** does not modify **SPH**!
- **ZPH** register: the zero page of the original 6502 is always located at \$0000..\$00FF. In VCPU the upper 8 bits of the address can be changed so the zero page can be relocated to an other memory page. This affect the zero page addressing modes only! In case of changed **ZPH** the direct addressed instructions (for example: LDA \$0080) always refer to the real address<sup>7</sup>!
- Handling of the CBM SERIAL, the serial bus is done by special “micro” instructions. By using them any kind of data transfer protocol can be programmed “by basic steps”. The execution time for most of these instructions are fixed so time critical transfers can be implemented too.

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<sup>7</sup> This is especially important for *Y-indexed* addressing modes because usually the instructions does not have a \$zp,Y addressing mode! But compilers will generate \$qwer ,Y addressing mode which – in case of relocated zero page – will not use the expected address.

### 3.3 Memory map for the emulated 6502

- \$0000..\$05FF / \$0000..\$0EFF: the memory buffers for file handles and RAM area for programs
- \$FC00..\$FCFF: the “command channel” of the drive can be read/written in this area but only in the length of the channel
- \$FD00..\$FDFF: the “error channel” of the drive can be read/written in this area but only in the length of the channel
- \$FE00..\$FEFF: I/O area, current length is 16 BYTES

### 3.4 I/O registers

- \$FE00: VCPU version number, read only. (Currently \$41, the same value that is present in the response of the “ZI” command.)
- \$FE01: Current device number of SD2IEC device (8..11), read only.
- \$FE02: State of SD2IEC buttons and LEDs, read/write. B0 = “BUSY LED”, B1 = “DIRTY LED”. 1: LED is on. B6 = “PREV BUTTON”, B7 = “NEXT BUTTON”. 1: button is depressed.
- \$FE03..\$FE04: Diagnostics, the function may change in the future, not usable!!
- \$FE05..\$FE09: unused, \$00
- \$FE0A: ATN / SRQ lines control, read/write. B7 = ATN, B6 = SRQ. For write the drive of the lines can be turned on/off for read the set state can be read back not the current state of the lines!
- \$FE0B: current state of ATN / SRQ lines, read only! B7 = ATN, B6 = SRQ.
- \$FE0C: CLK / DAT lines control, read/write. B1 = DAT, B0 = CLK. For write the drive of the lines can be turned on/off for read the set state can be read back not the current state of the lines!
- \$FE0D: current state of CLK / DAT lines, read only! B7 = DAT, B6 = CLK.
- \$FE0E: current state of CLK line, read only! B7 = CLK.
- \$FE0E: CLK line control, write only! B0 = CLK.
- \$FE0F: current state of DAT line, read only! B7 = DAT.
- \$FE0F: DAT line control, write only! B0 = DAT.

At address \$FE02 the LEDs on the device can be controlled. Not all devices contain both LEDs! There are SD2IEC hardware with only 1 LED, that can be controlled by the bit of “BUSY LED”. The LEDs can be programmed easily but the system calls (file open/close/etc.) can change them the usual way so their state is not guaranteed to be kept. (It’s useful to leave their control to the drive *firmware* “in normal use”). In case of error the usual “flashing LED” won’t work during the execution of a VCPU program!

The same \$FE02 address can be used to query the state of the two buttons. During a VCPU program execution the original functions of the buttons does not work! There is SD2IEC hardware without buttons! Therefore the use of these buttons is not recommended. The occasional disk image swap is possible in a programmed way but it's useful to do it in an automated way without user interaction.

In the range of \$FE0A..\$FE0F the control lines for the serial bus can be found. These registers won't be expanded in the future, the unused bits are guaranteed to return the value %0, any value can be written to the unused bits! The handling of the serial bus is possible using these registers but not recommended. For this task the VCPU has dedicated instructions.

## **4 CBM serial bus**

### **4.1 Hardware**

The lines of the serial bus are at logical high level when not in use. This high level can be pulled low by any device (computer / peripheral) attached to the bus. High level is possible on any lines of the bus when all of the devices turn off the pull low! Because of this in this document the term "driving the line" always means that the device pulls the line low and "releasing the line" means that the pulling low is switched off. In the latter case the high level can be present only when all of the devices "releases" that. (None of the devices can "force" a line to high level.)

### **4.2 Software**

Software can handle the lines of the serial bus as a bit of a peripheral register by. The "level" of the given line is shown by the appropriate peripheral bit. "Driving" and "releasing" the line is controlled by toggling a bit of a different peripheral. On the SD2IEC side the peripheral bit always shows the actual logical level of the lines (for a low level line %0, %1 for high level), controlling the output is done the same way (%0 pull low, %1 releases).



### 4.3 Lines

Serial bus has 4 lines relevant for programming. These (and their original functions) are:

- SRQ: Service ReQuest. Not used. This line should be driven by peripherals, it's input on computer. In 1541 this line is not connected. In VIC20 one of the VIAs receive it. The CPU can't read it's real level but the change can generate an interrupt. In the C64 it work the same: one of the CIAs receive it and an interrupt can be generated. It's not connected in the C16 / C116 / plus/4 computers. On the C128 the "fast serial bus" mode uses it but drive *firmware* does not support it yet. Controlling the SRQ line by VCPU is currently not implemented! On most of SD2IEC hardware – as it's not used – controlling the line is not implemented!
- ATN: ATtention: call for device addressing. This line is controlled by the computer, it's input on peripherals. At low level the device addressing is done, this is the time when the computer selects the peripheral to communicate to. In 1541 this is input only it's change controls turning on driving DAT. SD2IEC – unlike CBM peripherals – can drive it and it can be controlled by VCPU. On VIC20, C64, C16 / C116 / plus/4 and C128 the line is output only, the state of the line cannot be read back! Driving by SD2IEC can be useful when the communication is directly between peripherals without including a computer.
- CLK: CLock: the "clock" of the data transfer, this helps to synchronize the transferred bits. Can be driven by both computers and peripherals.
- DAT: DATA: the transferred data bit. Can be driven by both computers and peripherals.

## 5 VCPU instruction set

The VCPU instructions can be divided to 3 groups: the original 6502 instructions, the extended functions' instructions and the serial bus handler "micro" instructions. The documentation for the instructions in the first group can be found in the well known documentations about programming the 6502.

### 5.1 Instructions of the extended functions

Mnemonic	Op-code	Registers <sup>8</sup>	Description
TYSPH	\$D4	SPH	Transfer Y to SPH register
TSPHY	\$F4	Y, N, Z	Transfer SPH to Y register
LDSPH #\$xx	\$22 \$xx	SPH	LoaD SPH register

- TYSPH: moves value of register **Y** to register **SPH**
- TSPHY: moves value of register **SPH** to register **Y**
- LDSPH #\$xx: loads the value to register **SPH**

TYZPH	\$44	ZPH	Transfer Y to ZPH register
TZPHY	\$54	Y, N, Z	Transfer ZPH to Y register
LDZPH #\$xx	\$02 \$xx	ZPH	LoaD ZPH register

- TYZPH: transfers value of register **Y** to register **ZPH**
- TZPHY: transfers value of register **ZPH** to register **Y**
- LDZPH #\$xx: loads the value to register **ZPH**

Registers **SPH** / **ZPH** must point to RAM area! On an attempt to write a value that points outside of RAM the program execution is interrupted with an error code.

BTASC	\$E2	A, X, Y	Binary To ASCii conversion
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- BTASC: VCPU does not support BCD mode but sometimes a number's decimal representation is needed. BTASC converts accumulator to the 3 characters 000..255. The registers **Y:X:A** (in this order) will contain the resulting decimal digits. Status register is not modified!

<sup>8</sup> N, V, B, D, I, Z, C characters denote the bits of the status register, A, X, Y, SP, SPH, ZPH refers to CPU registers.

## 5.2 Serial bus handling “micro” instructions

Most of these instructions do not change the status register’s bits! Execution times are fixed, the unit is 1 clock period of the 1MHz 6502 in the 1541. (1 6502 clock cycle is “1T”.)

Mnemonic	Op-code	Time	Registers	Description
UWATL	\$43	1.5T+	–	Wait for serial ATN line Low
UWATH	\$53	1.5T+	–	Wait for serial ATN line High
UWCKL	\$23	1.5T+	–	Wait for serial CLK line Low
UWCKH	\$33	1.5T+	–	Wait for serial CLK line High
UWDTL	\$03	1.5T+	–	Wait for serial DAT line Low
UWDTH	\$13	1.5T+	–	Wait for serial DAT line High

- UWATL: Waits for serial bus line ATN low level
- UWATH: Waits for serial bus line ATN high level
- UWCKL: Waits for serial bus line CLK low level
- UWCKH: Waits for serial bus line CLK high level
- UWDTL: Waits for serial bus line DAT low level
- UWDTH: Waits for serial bus line DAT high level

These instructions wait for the desired level of the serial bus lines. If the line is already at the waited level before beginning of the instruction execution then execution time will be 1.5T. Waiting will be finished in less than 1T after the line reached the watched level and the execution continues.

USATL	\$C3	1.5T	–	Set serial ATN line to Low
USATH	\$D3	1.5T	–	Set serial ATN line to HighZ
USCKL	\$A3	1.5T	–	Set serial CLK line to Low
USCKH	\$B3	1.5T	–	Set serial CLK line to HighZ
USDTL	\$83	1.5T	–	Set serial DAT line to Low
USDTH	\$93	1.5T	–	Set serial DAT line to HighZ

- USATL: Sets serial bus line ATN to low
- USATH: Releases serial bus line ATN
- USCKL: Sets serial bus line CLK to low
- USCKH: Releases serial bus line CLK
- USDTL: Sets serial bus line DAT to low
- USDTH: Releases serial bus line DAT

These instructions control the serial bus lines. “Releasing the line” is done only on the SD2IEC side, other devices can still hold it at low level!

UCLDL	\$0B	1.5T	-	Set serial CLK to Low / DAT to Low
UCLDH	\$1B	1.5T	-	Set serial CLK to Low / DAT to HighZ
UCHDL	\$2B	1.5T	-	Set serial CLK to HighZ / DAT to Low
UCHDH	\$3B	1.5T	-	Set serial CLK to HighZ / DAT to HighZ

- UCLDL: Sets serial bus lines CLK and DAT to low
- UCLDH: Sets serial bus line CLK to low and releases DAT
- UCHDL: Releases serial bus line CLK and sets DAT to low
- UCHDH: Releases serial bus lines CLK and DAT

With these instructions the serial bus CLK and DAT lines can be controlled in a single step.

UATCK # $\$xx$	\$6B $\$xx$	2T	-	Copy A register bit To CLK line
UCKTA # $\$xx$	\$7B $\$xx$	2T	A	Copy CLK line to A register bit
UATDT # $\$xx$	\$4B $\$xx$	2T	-	Copy A register bit To DAT line
UDTTA # $\$xx$	\$5B $\$xx$	2T	A	Copy DAT line To A register bit

- UATCK # $\$xx$ : Drives/releases the CLK line based on the selected bit of register A
- UCKTA # $\$xx$ : Copies the state of CLK line to the selected bit of register A
- UATDT # $\$xx$ : Drives/releases the DAT line based on the selected bit of register A
- UDTTA # $\$xx$ : Copies the state of DAT line to the selected bit of register A

The parameter of the instructions is a bitmask where only a single bit can have the value %1! Reading CLK / DAT the value of the line is copied to that bit of accumulator where the %1 is present in the bitmask parameter. On write driving/releasing the state of the line will be set based on the bit of accumulator where the bitmask value is %1. Attention: VCPU SR bits does not change on accumulator value change!

UATCD # $\$xx$ , # $\$yy$	$\$8B$ $\$xx$ $\$yy$	2.5T	-	Copy <b>A</b> register bits To CLK / DAT
UCDTA # $\$xx$ , # $\$yy$	$\$9B$ $\$xx$ $\$yy$	2.5T	A	Copy CLK / DAT line To <b>A</b> register bits

- UATCD # $\$xx$ , # $\$yy$ : Controls the CLK/DAT lines based on bits of register **A**
- UCDTA # $\$xx$ , # $\$yy$ : Copies the state of CLK/DAT lines to the selected bits of register **A**

The parameters of the instructions are two bitmasks, both of them with a single %1 bit! The first bitmask belongs to the CLK line and the second to DAT. On read the state of CLK will be written to the bit of accumulator where the %1 value is present in the first bitmask and the state of DAT likewise with the second bitmask. On write the first bitmask controls driving/releasing CLK and the second control DAT. Attention: VCPU **SR** bits are not affected even when value of accumulator is changed!

These instructions are restricted to parameter values where only one bit is %1. (So  $\$01$ ,  $\$02$ ,  $\$04$ ,  $\$08$ ,  $\$10$ ,  $\$20$ ,  $\$40$ ,  $\$80$ .) Result of other bit combinations is “undefined”. (On read when multiple bits are %1, the selected line will be copied to all bits with %1 value in the mask. Probably this won’t change in the future. On write when multiple bits are %1 then some logical combination of accumulator bits will determine the state of the line that can depend on the hardware version of SD2IEC so it’s not recommended to use “illegal” bitmasks.) On instructions that read/write two lines the two bitmasks cannot be the same! (On read it’s “undefined” which line’s state will be copied to accumulator. On write both lines’ state will be set based on the same bit of accumulator, most probably this won’t change in the future.)

ULBIT	$\$DB$	2T	N, V, Z	Lines BIT test
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- ULBIT: Copies the current state of the serial lines to the bits of the status register

This instruction copies the current state of the serial lines to the bits of the status register: ATN goes to V, CLK goes to N, and DAT goes to Z. The conditional jumps after the instruction will do the jump based on the state of the checked line. (BVS / BVC: ATN line high / low, BMI / BPL: CLK line high / low, BEQ / BNE: DAT line high / low.)

USND1	\$63	?T		Send <b>A</b> register to DAT, 1 bit mode
URCV1	\$73	?T	A	Receive from DAT to <b>A</b> register, 1 bit mode
USND2	\$E3	?T		Send <b>A</b> register to CLK/DAT, 2 bit mode
URCV2	\$F3	?T	A	Receive from CLK/DAT to <b>A</b> register, 2 bit mode

- USND1: 1 bit synchronized data send
- URCV1: 1 bit synchronized data receive
- USND2: 2 bits synchronized data send
- URCV2: 2 bits synchronized data receive

The “1 bit” instructions implement sending/receiving of 1 BYTE synchronized data using CLK / DAT lines. Synchronization is done by line CLK which is toggled by the computer and the drive responds to it’s changes. Because of this the execution time is undefined, depends on the speed of the computer:

- The USND1 instruction is for sending data. At first it switches off driving of line CLK then waits for it’s high level. When CLK is high it copies the value of bit 0 of register **A** to DAT. After that it wait for low level of line CLK. When the computer received B0 it switches CLK to low. In response the drive copies bit 1 of register **A** to DAT and waits for CLK to be high. When the computer received B1 it releases CLK. Then the drive puts the next bit to DAT and so on. At the end of the BYTE the computer sets CLK to low and the drive puts bit 7 of register **A** to DAT and the instruction terminates and the next one can begin.
- The URCV1 instruction is for receiving data. At first it switches off driving of lines CLK / DAT then waits for CLK low level. The computer copies B0 of the data to be sent to DAT and switches CLK to low. In response the drive reads DAT to bit 0 of register **A** then waits for CLK high. The computer sets B1 to DAT then toggles CLK to high. Then the drive reads DAT to bit 1 of register **A** and so on. At the end of the BYTE the computer copies bit 7 to DAT and releases CLK then the drive reads B7 to register **A** and the instruction terminates and the next one can begin.

The “2 bits” instructions use lines ATN / CLK / DAT to implement synchronized sending / receiving of a whole BYTE. The synchronization is done with line ATN which is toggled by the computer and the drive reacts to it’s changes. Because of this the execution time is undefined, depends on the speed of the computer:

- The USND2 instruction is for sending data. At first it switches off driving ATN then waits for it’s high level. When ATN is high it copies bit 1 of register **A** to DAT and bit 0 to CLK. Then waits for ATN low level. When the computer received B1/B0 it toggles ATN to low. In response the drive copies bit 3 of register **A** to DAT and bit 2 to CLK then waits for ATN high level. When the computer received B3/B2 it releases ATN. Then the drive puts the next bit pair to DAT/CLK and so on. At the end of the whole BYTE the computer toggles ATN to low and in response the drive puts bits 6 / 7 of register **A** to CLK/DAT and the instruction terminates and the next one can begin.

- The URCV2 instruction is for receiving data. First it switches off driving ATN / CLK / DAT lines and waits for ATN low. Computer puts B0 of data to DAT and B1 to CLK then sets ATN to low. The drive reads DAT to bit 0 of register **A** and CLK to bit 1 and waits for ATN high. Computer sets B2 to DAT and B3 to CLK then sets ATN to high. The drive reads DAT to bit 2 of register **A** and CLK to bit 3 and so on. At the end of the BYTE the computer copies bits 6 / 7 to DAT / CLK lines and releases ATN. Then drive reads DAT to B6 of register **A** and CLK to B7 and the instruction terminates and the next one can begin.

UINDB \$offs	\$AB \$of	1.5T/2T	X, Y	INcrement <b>X</b> , Decrement <b>Y</b> , Branch if no cy.
UDEDDB \$offs	\$BB \$of	1.5T/2T	X, Y	DEcrement <b>X</b> , Decrement <b>Y</b> , Branch if no cy.

- UINDB \$offs: increment **X**, decrement **Y** and jump when **Y** did not became \$FF
- UDEDDB \$offs: decrement **X**, decrement **Y** and jump when **Y** did not became \$FF

These instructions increase or decrease the value of register **X**. Then decrease the value of register **Y**. When that underflow from \$00 to \$FF the execution continues with the next instruction. In this case the execution time is 1.5T. When **Y** did not become \$FF execution will jump to the parameter of the instruction and the whole execution time will be 2T. (The destination address is calculated in the same way as for all 6502 conditional jumps: the parameter is treated as a signed value in the range of -128..+127 and added to PC). Crossing a 256 BYTE page boundary does not affect the execution time. Attention: the VCPU **SR** bits are not affected by the execution of these instructions!

UDEL1	\$EA	1T	-	1T DELay
UDELY #\$xx	\$FB \$xx	1.5T+	-	DELaY

- UDEL1: 1T delay
- UDELY #\$xx: 1.5T + \$xx × 0.5T delay

UDEL1 instruction is 1T delay. (This is the opcode of NOP on the original 6502, execution time: 1T). UDELY is a delay instruction where the time is specified by the fixed value in the parameter. The shortest time is 1.5T. That is extended with the parameter value × 0.5T.

There are two additional data movement instructions:

LDA \$zp,X	\$B5 \$zp	2T	A,N,Z	Load Accumulator from zero page X indexed
STA \$zp,X	\$95 \$zp	2T	-	Store Accumulator to zero page X indexed

These are the original 6502 **X** indexed zero page read / write instructions but their execution time is 2T. As the VCPU zero page can be relocated anywhere (within the memory) they can read / write the whole memory.

### 5.3 Call drive *firmware* functions

Mnemonic	Op-code	Registers	Description
BREAK #\$xx	\$00 \$xx	A,X,Y	System Call

- BREAK #\$xx: call system function number \$xx

This is the BRK instruction of the original 6502. The instruction and the following byte is processed by directly drive *firmware* instead of the VCPU. The VCPU state is saved and the system call is processed.

## 6 System calls

With the BREAK #\$xx instruction various drive *firmware* functions can be accessed. The parameter is the number of the system function. The program execution will be suspended when the function requires stopping the CPU emulation. For other tasks the emulated 6502 code execution continues from the address after the parameter of the BRK + parameter instruction. The system call will put its return values in VCPU **A / X / Y** registers so their contents are not preserved! The bits of the status register are not set by the value of any of the registers, the returned values must be checked!



## 6.1 Codes of system calls

Code	Referenced name	Description
\$00	SYSCALL_EXIT_OK	Exit with messages “00, OK,00,00”
\$01	SYSCALL_EXIT_SETERROR	Exit with selected message
\$02	SYSCALL_EXIT_FILLEDERROR	Exit with “error channel” filled
\$03	SYSCALL_EXIT_REMAIN	Exit without modifying the “error channel”
\$11	SYSCALL_DISABLEATNIRQ	Disables the ATN active VCPU exit
\$12	SYSCALL_ENABLEATNIRQ	Enables the ATN active VCPU exit
\$13	SYSCALL_SETFATPARAMS	Set FAT file handling parameters
\$21	SYSCALL_DIRECTCOMMAND	Execute command from “command channel”
\$22	SYSCALL_DIRECTCOMMAND_MEM	Copy command from memory to “command channel” and execute it
\$23	SYSCALL_OPEN	Open file (name in “command channel”)
\$24	SYSCALL_OPEN_MEM	Open file (name in memory)
\$25	SYSCALL_CLOSE	Close file
\$26	SYSCALL_CLOSEALL	Close all open files/channels
\$27	SYSCALL_REFILLBUFFER	Refill buffer for reading/empty for write
\$28	SYSCALL_GETCHANNELPARAMS	Query channel parameters
\$31	SYSCALL_CHANGEDISK	Request change disk

## 6.2 Description of system calls

- \$00: SYSCALL\_EXIT\_OK: Terminate VCPU program execution. The contents of the “error channel” will be “00, OK,00,00” and the computer will be able to handle the peripheral in the usual way.
- \$01: SYSCALL\_EXIT\_SETERROR: Terminate VCPU program execution. The contents of the “error channel” will be set to the required message! Before the system call register **A** must contain the error code and registers **X** / **Y** must contain the track / sector numbers. Only existing error codes are allowed!
- \$02: SYSCALL\_EXIT\_FILLEDERROR: Terminate VCPU program execution. The “error channel” must be filled and **X** must contain the number of bytes put in error channel. After that the system function can be called.
- \$03: SYSCALL\_EXIT\_REMAIN: Terminate VCPU program execution. Without changing the contents of the “error channel”. (When a previous function returned with error using this function to terminate VCPU code execution the computer will be able to query the error in the usual way)
- \$11: SYSCALL\_DISABLEATNIRQ: The default behavior is to interrupt VCPU code execution when ATN goes active. This can be switched off with this system call when the ATN is required for other purposes.

- \$12: SYSCALL\_ENABLEATNIRQ: Turns back on the interrupt of VCPU code execution for ATN active.
- \$13: SYSCALL\_SETFATPARAMS: drive *firmware* reads / writes files in 254 byte block in case of the FAT filesystem, just like as in a disk image. This system call can change this behavior. Before the call register **X** must contain the starting position in within the data buffer (default is 2, this is the start for loaded data), and register **Y** contains the number of bytes to be read in one step (default value is 254). 0 means 256 BYTES! After the system call registers **X** / **Y** will contain the values set. If the starting position plus BYTE count is higher than the size of the data buffer (256), the setting will not be applied! After return the registers will contain the actual values so with “bad” parameters the current settings can be queried.
- \$21: SYSCALL\_DIRECTCOMMAND: The computer can communicate the tasks to the drive via the “command channel”. (Delete file, change directory, etc.) VCPU can execute commands in the same way: the “command channel” is mapped in the memory of the 6502. The commands bytes must be written here directly. The number of bytes in the “command channel” must be set in register **X** and the system function can be called. drive *firmware* will try to execute the command then returns to the VCPU program execution. After the system call register **A** will contain the error code from the “error channel” and register **X** will contain the number of bytes in the “error channel”.
- \$22: SYSCALL\_DIRECTCOMMAND\_MEM: This command is the same as the previous one (number \$21) but before execution the command will be copied from the VCPU memory to the “command channel”. Before call register pair **ZPH:Y** must be set to the starting address of the command and register **X** must be set to the number of bytes to be copied (the length of the command). Return values are the same as for command \$21.
- \$23: SYSCALL\_OPEN: Open file. The “command channel” must contain the name and open mode of the file, register **X** must be set to the length of the filename. Register **A** must be set to the number of the requested channel which must be between 0..14. After return register **A** will contain the error code from the “error channel”, register **X** will contain the number of bytes written to the “error channel”. Register **Y** will contain the *number* of the data buffer associated with the file. This value is the upper 8 bits of the VCPU memory. For example number \$02 means that the buffer is at \$0200..\$02FF in the memory! Additionally in the “error channel” memory (\$FDxx) three additional data can be found: starting position of data in the buffer (\$FD60), position of the last used BYTE (\$FD61), and a flag signaling if there is data left in the file (\$FD62).
- \$24: SYSCALL\_OPEN\_MEM: This command is the same as the previous one (number \$23) but before execution copies the file name from the VCPU memory to the “command channel”. Before call the address of the memory must be set in register pair **ZPH:Y**, in register **X** the number of bytes to be copied (length of the filename). Register **A** must contain the number of the requested channel just like with command \$23. Returned values are the same as there.
- \$25: SYSCALL\_CLOSE: Close File / channel. Register **A** must contain the channel number specified for OPEN then call the system function. In case of successful execution register **A** will contain \$00.
- \$26: SYSCALL\_CLOSEALL: Close all open files / channels. There are no parameters and return values.

- \$27: SYSCALL\_REFILLBUFFER: For file read this system call can be used to request loading of the next set of bytes. Register **A** must contain the number of the channel specified for OPEN the call the function. The returned parameters are the same as for commands \$23 / \$24: SYSCALL\_OPEN (\_MEM). For file write when the data buffer is full or no more bytes need to be written register **X** must contain the starting position in the buffer and register **Y** must contain the position of the last used byte. Register **A** is the number of channel used for OPEN. The returned parameters are the same as for command \$23 / \$24: SYSCALL\_OPEN (\_MEM).
- \$28: SYSCALL\_GETCHANNELPARAMS: Query channel parameters. Register **A** must be set to the number of the channel to be queried. Returned parameters are the same as for commands \$23 / \$24: SYSCALL\_OPEN (\_MEM).
- \$31: SYSCALL\_CHANGEDISK: “Disk change” function of drive *firmware*. Using this function the disk images can be swapped based on the contents of an external swap list file. Register **X** must be filled with the number of the disk image. Register **A** will be set to \$00 on successful disk change. To use this function the swap file must be set for drive *firmware* (AUTOSWAP.LST). When the user chooses image with the buttons on the SD2IEC device this change will be done automatically. The swap file can be mounted without user interaction using the “XS:AUTOSWAP.LST” command. (See drive *firmware* documentations)

## 7 VCPU program execution error handling

VCPU program execution can terminate for several reasons beside “SYSCALL\_EXIT\_XX” system calls. When a system call with an unknown code is made a “97,VCPU ERROR,101,XX” error will be set where XX is the code of the unknown system function. For other terminate reasons the result will be “97,VCPU ERROR,100,XX” where XX will be the same as the **INT** parameter of the “ZC” command. The bits of this BYTE mean different events:

- B7: drive *firmware* compilation error. The programmer / user should not encounter this one. It means the firmware is not properly compiled.
- B6: Address error. When the VCPU would jump to an unavailable address the execution will be terminated with this signal.
- B5: Address error. The system call was made from an invalid address.
- B4: Invalid instruction. Execution “illegal” opcodes will be terminated with this signal.
- B3: SD card has been removed (or inserted if there was no card inserted previously).
- B2: Program execution is terminated due to ATN active. This can be disabled with the proper system calls!
- B1: Read / write address error. When the VCPU would read / write outside of the usable memory / I/O buffers the execution will be terminated with this signal.
- B0: Program execution is terminated due to system call. This will be set for exit system calls.

## 8 Remarks

### 8.1 1 bit / 2 bits

A lot of users does not use the SD2IEC drive as a single drive, they have a 15x1 drive connected too. The basic operation of the serial bus that in response to the computer's ATN active signal the peripherals pull the DAT line to low. Because of this the programs that use ATN for data transfer can be used only when there is only one peripheral on the serial bus! For these cases the SD2IEC drives provide a feature to "disconnect" them from the serial bus without actually plugging them off. It's important to note that in case of the original 15x1 drives this is not possible! (Turning off the drive is not enough, the drives must be plugged off!) Due to this behavior the SD2IEC transfer routines should be implemented to use ATN in very justified cases! Of the above, *synchronous transfers* the 1 bit versions does not use ATN. Preferred communication protocols use CLK / DAT only!

### 8.2 Buffers / memory

The VCPU program memory is part of the drive *firmware* data buffers. For this reasons the programmer must be careful to not putting program code to the buffers used by file operations because they will be overwritten. The programmer (currently) can't control which operation will use which buffer but – fortunately – the buffer allocation / freeing is reliable. The drive *firmware* is allocating buffers from the beginning, in order but there are some thing to be considered. When the user (or the program itself) uses disk images the drive will allocate a buffer to handle that "internally". In generic uses cases this will be buffer 0. This buffer remains allocated after the user "exits" that disk image! In addition the opened file allocates a buffer too which in this case will be buffer 1. But if this file is not inside a disk image and the user haven't used a disk image yet this will be buffer 0! For this reason the number of the buffer used should be handled dynamically.

These two buffers will be the VCPU memory range \$0000..\$00FF and \$0100..\$01FF. Because of this the zero page and the stack must be relocatable and the VCPU supports this. The remaining memory for the drives with few buffers is scarce, 1 KBYTE which is half of the memory of the 1541. But the disk handling functions are provided by the drive *firmware* so the complex (and thus memory intensive) program codes are not required here.

Number of buffers is determined by the amount of RAM in the SD2IEC drive's microcontroller. As this was not really relevant before most of the users have an SD2IEC drive which allows 6

buffers only. Because of this the programmer should be prepared for this number. When more memory is required the users won't have the hardware to support that so they won't be able to run that program.

### 8.3 Disk images / Directories

The different disk images can be accessed as simple directories with the drive *firmware*. Changing directories are done with the “CD: . . .” command. (See drive *firmware* documentation for more details.) In addition switching between directories / disk images is also possible using “AUTOSWAP.LST” (or any other, manually specified) file. (In normal operation stepping between the disk images / directories in the list is done by using the device buttons. During a VCPU program execution the SYSCALL\_CHANGEDISK (\$31) function is also possible) Important: during **directory / disk image change all the open file / communication channel gets closed!** When a communication channel was open for the sector level handling of a disk image it must be reopened after the disk swap!

### 8.4 Storage speed

Although most of the load (save) time is made of the communication between drive ↔ computer but time for accessing the SD card and handling its file system is not negligible. But these times depend on the type of the card the parameters of the file system, the location of the file, etc. The programmer must not assume that the times experienced during development will be met by the configuration of every user!

### 8.5 VCPU extended / “micro” instruction codes

Due to the few resources of the hardware of the most popular SD2IEC drives compatibility with an old CBM drive is not a goal. Because of this 100% compatibility of the CPU emulation with the original 6502 is also not required. Support for the “undocumented” instructions is missing for this very reason but the usability of this instructions is also limited. Because it does not need to be compatible with an existing hardware it would be useful to implement the additional instructions / addressing modes of the 65C02 CPU instead of the “undocumented” instructions. The codes of the VCPU extra instructions has been selected to occupy the places of the unused instructions of the 65C02 CPU so later this processors new instructions / addressing modes can be implemented! (Currently there is not enough free place for devices with smaller memory.)

## 9 About the sample sources

### 9.1 The “#”

The VCPU has several new instructions in addition to the original 6502. These instructions mostly use *immediate* addressing mode. This addressing mode is marked by “#” in the original 6502 *assembler* syntax (e.g. # $\$55$ ), in the previous parts of the documentation these instructions are also presented this way. Currently there is no *assembler* supporting VCPU extended instructions, so a macro definitions source has been created to support using them. However the *assemblers*’ macro definitions usually can’t process a parameter which is *number* (or a label representing it) and begins with the symbol “#”! For this reason these instructions, defined as macros the “#” symbol is left out from the parameters. So they are written as

BREAK  $\$00$  instead of BREAK # $\$00$

form. But this does not mean that the parameter of these instructions is a (zeropage) address! As all of the “new” instructions has only one addressing mode this won’t cause a misunderstanding. If in the future there will be an *assembler* supporting these instructions directly then the original syntax using “#” should be implemented but for compatibility reasons the one without the “#” can be accepted too.

### 9.2 Supported architectures for the sample programs

The sample programs can be compiled for 4 different architectures. These are VIC20, C64, C16 / C116 / plus/4 (C264 series) and C128. The KERNAL level programming of these machines are the same but there are programs which demonstrate the data transfer between the drive and the computer and these are hardware dependent. The purpose of the samples is rather demonstrate the SD2IEC + VCPU than the programming of the computer so – to keep it simple – the VCPU sources are the same for all platforms. This also means that a sample showcasing the data transfer is not optimal for all platforms! (For example the computer hardware would require different bit order for every platform). (Ones of) The goal(s) of these samples is to aid the programmer to implement the optimal data transfer for the chosen platform.

### 9.3 License for the sample programs

The sample programs are made because they can be helpful. Knowing the “**there is no guarantee for anything, not even basic operations**” remark they can be used, wholly or partially freely, without restrictions.

## 9.4 Description of the sample programs

The sample programs are made to test the VCPU extension functions but they can be useful to answer questions about programming the device. All of the programs begin with checking the peripherals of the computer, counting the number of them connected to the serial bus. Then it searches the SD2IEC drive (when there are more it chooses the last one) and does its tasks with this drive. The functions of these programs are the following:

- **A-DETECT:** Prints the long version (“X?”) of the found drive. Check for VCPU support (“ZI”) and displays the response. After that it prints the number of buffer (“ZB”) and the current state of the VCPU (“ZC”).
- **B-SHOWMEM:** Displays the memory handled by the SD2IEC VCPU extension (“ZR”).
- **C-PRINTIO:** Displays the I/O area visible for the VCPU. This (and the rest of the samples) requires a program to be downloaded to the drive.
- **D-BUTTLED:** The two LEDs of the SD2IEC (“BUSY” / “DIRTY”) can be controlled by the two buttons (“PREV” / “NEXT”). In addition the computer’s CLK / DAT lines also control these LEDs (C + V and D + F keys). At exit it queries the drive status which requires ATN activity causing the VCPU to interrupt execution. Because of this the status will display the matching error code. After this the VCPU state is also displayed.
- **E-SR1B-PIO:** The computer send 256 BYTEs to the SD2IEC then the drive sends this packet back to the computer. It checks if it’s the same as it was sent. If they match the sending begins anew. This test runs until the user exits or there is a comparison mismatch. The received data is displayed on the screen. This test uses CLK / DAT lines only. DAT is used for transferring data bits and CLK is used by the computer for timing the transfer. The VCPU side of the communication is implemented using the I/O registers in the “old fashioned” way. This transfer mode is not recommended!
- **F-SR1B-USR:** Data transfer test. The transferred data is the same as the one described for E-SR1B-PIO. This one also uses CLK / DAT only. The VCPU side implementation uses USND1 / URCV1 instructions. This is a recommended method!
- **G-SR1B-URE:** Data transfer test. The transferred data is the same as the one described for E-SR1B-PIO. This one also uses CLK / DAT only. The VCPU side implementation uses UDTTA / UATDT instructions. This is a recommended method! The order of the bits on the DAT line is reversed compared to the previous transfer protocols.
- **H-RECVTIME1B:** Data receive test, receives and checks a specified number of BYTEs for every frame. Uses CLK / DAT lines only.
- **I-SR2B-PIO:** Data transfer test, the two bit equivalent of E-SR1B-PIO. In one step 2 bits are moved on the CLK / DAT lines and the ATN is used for timing. For two bit transfers using ATN only one drive (in this case the SD2IEC) can be connected to the serial bus of the computer! The VCPU side of the communication is implemented using the I/O registers. This transfer mode is not recommended!
- **J-SR2B-USR:** Data transfer test, the two bit equivalent of F-SR1B-USR. The data transfer is the same as described for I-SR2B-PIO. The VCPU side implementation uses USND2 / URCV2 instructions. This is a recommended method!



- K-SR2B-URE: Data transfer test, the two bit equivalent of G-SR1B-URE. The VCPU side implementation uses UCDA / UATCD instructions. This is a recommended method! The order of the bits on the DAT line is reversed compared to the previous transfer protocols.
- L-RECVTIME2B: Data receive test, the two bit equivalent of H-RECVTIME1B.
- M-LOADTST1B: File load test. 1 bit data transfer using CLK / DAT lines. There must be an SD card in the drive with the test file "TSTDAT2M.SEQ" in the current directory. This is a 2 MBYTES file consisting of random numbers. The test reads this file four times. The difference between reads are block size (254 or 256 BYTES) and the presence of checksum (calculated or skipped). The process measures "time" for reading. (The "time" is the number of interrupts for the used platform which is ~60 for VIC20 / C64, for (PAL) C16 / C116 / plus/4 and (PAL) C128 is ~50 per second. If the counted value is divided by this number the load time can be calculated. The values directly not applicable to compare platforms!
- N-LOADTST2B: File load test. The two bit equivalent of M-LOADTST1B using CLK / DAT and ATN lines.
- O-DISKIMGS: Disk image handling test. There must be an SD card in the drive with the "VCPUTSTDSK1.D64" and "VCPUTSTDSK2.D64" disk images in the current directory. The test enters the first then the second disk images using "CD: . . ." command. Then reads the 3-3 files in them with direct sector read commands. It calculates a checksum of the files which is (among other data) is returned to the computer which displays / checks them.
- P-AUTOSWAP: Disk image handling test. The tests described for O-DISKIMGS will be processed but the disk change is performed using the "AUTOSWAP.LST" file. (This one is also required in the current directory of the SD card besides the disk images).
- Q-BENCHMARK: File read speed test. The VCPU test program reads the "TSTDAT2M.SEQ" test file used by the load tests using drive *firmware* and the computer measures the read "time". It repeats this with both 254 and 256 BYTES block size. This test is used for testing the "raw" file read performance of the drive! The measured "time" is calculated in the same way as for file load tests.
- Y-LINEDIAG: Test of the serial lines' state from the SD2IEC side. Diagnostics program, may be removed in the future!
- Z-VCPUCTST: Test for the VCPU core. Checks for running the emulated 6502 instructions. Not a full, "comprehensive" test! Currently all (original 6502 and extended) instructions are run / tested with at least one addressing mode. ("Micro" instructions are not tested here, most of them are tested in the data transfer tests.) The occasional VCPU instruction errors may get a dedicated test in this program together with their fixes.

## 10 Known bugs

- VCPU program execution allows only from RAM area! But address of the instruction to be executed is checked only for unconditional jumps. This can cause that during a simple program execution the **PC** can run out of the area designated as RAM. Additionally the conditional jumps can lead to jumping out of allowed memory range. In these cases the operation is “undefined”. Write to an invalid memory address is not executed (just like in case of normal program execution) so this does not affect normal operation of the drive *firmware*. System function calls (\$00: BREAK code) from these invalid addresses are also not executed.
- The traditional interrupt handling is missing! Instead of that there are several events that interrupt VCPU program execution (such event is for example removal of the SD Card). These events are not checked after execution of every instruction just after the ones that allow creating program loops. (These are typically the jump / wait “micro” instructions.) Because of this the program is not interrupted when the event is happening but after one of the following jump instructions! In these cases the VCPU status query value of **PC** won't reflect the actual instruction when the event happened.
- Execution time of instructions accessing the I/O area depends on the address of the register. Accessing the same register always takes the same time, independently of the written / read data.
- BTASC instruction converts binary values to ASCII characters using simple cycles so execution time (only for this instruction) depends on the value to be converted! For timing critical codes this instruction must be avoided.
- Execution times for the original 6502 instructions are not defined (with several exceptions). Possible optimizations can change them in the future!

# Table of contents

1 Introduction.....	2
1.1 Goals.....	2
1.2 Differences compared to programming the original Commodore drives.....	2
1.3 License.....	2
2 Commands available for the computer.....	3
2.1 “ZI”: Query VCPU information.....	3
2.2 “ZB”: Query data buffer state.....	4
2.3 “ZR”+ADDRLO+ADDRHI+LENGTH: Read data buffers as memory.....	4
2.4 “ZW”+ADDRLO+ADDRHI+BYTE1+...: Write data buffers as memory.....	4
2.5 “ZE”+ADDRLO+ADDRHI+...: Execute program using VCPU.....	5
2.6 “ZC”: Query VCPU state.....	5
3 The VCPU.....	6
3.1 Major differences.....	6
3.2 VCPU extended functions.....	6
3.3 Memory map for the emulated 6502.....	7
3.4 I/O registers.....	7
4 CBM serial bus.....	8
4.1 Hardware.....	8
4.2 Software.....	8
4.3 Lines.....	9
5 VCPU instruction set.....	10
5.1 Instructions of the extended functions.....	10
5.2 Serial bus handling “micro” instructions.....	11
5.3 Call drive <i>firmware</i> functions.....	16
6 System calls.....	16
6.1 Codes of system calls.....	17
6.2 Description of system calls.....	17
7 VCPU program execution error handling.....	20
8 Remarks.....	21
8.1 1 bit / 2 bits.....	21
8.2 Buffers / memory.....	21
8.3 Disk images / Directories.....	22
8.4 Storage speed.....	22
8.5 VCPU extended / “micro” instruction codes.....	22
9 About the sample sources.....	23
9.1 The “#”.....	23
9.2 Supported architectures for the sample programs.....	23
9.3 License for the sample programs.....	23
9.4 Description of the sample programs.....	24
10 Known bugs.....	26